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POWER THE FUTURE

AN006

Application Note

InnoGaN Layout Design Guide

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1. Overview

Compared with traditional silicon meterial, gallium nitride (GaN) can withstand larger electric fields in a smaller size while providing faster switching speed. Because of the inherent characteristics of high voltage and current slew rate (dv/dt and di/dt), , GaN devices are more susceptible to parasitic parameters such as parasitic inductance in practical applications when compared with Si power devices.

In order to take fully advantages of high speed switching for GaN devices while avoiding the impact of parasitic parameters, it is particularly important minimize the parasitic effects in layout design.

2. Key points in layout design

The common-source inductance, power loop, and gate driving loop are the three main aspects that affect the performance of GaN devices, which should be pay special attention to in the layout design of GaN.

2.1. Common-source Inductance(CSI)

2.1.1. Impact of CSI

Common-source inductance (CSI) is the loop parasitic inductance shared in the gate driving loop and the power loop.

During the switching process of the device, the CSI will generate a negative voltage adding on the gate driving voltage, which tends to hold back the gate voltage rising and slows down the switching process, thus increasing the switching losses. Table 1 shows the simulation results comparison of the switching loss of one of InnoGaN low-voltage product at drian current of 20A. The CSI increases from 0 nH to 0.1 nH in LTspice. The simulation results show that CSI has a great influence on the switching loss.

When the high side GaN is turned on in the half-bridge circuit as shown in Figure 1, the low side GaN will generate a negative induced voltage on its CSI due to the reduction of the freewheeling current. This negative voltage leads to a undershoot on the source node voltage, thus an overshoot on the gate-source voltage of low-side GaN, which may cause a fault turn on and the risk of short-through. Therefore in order to reduce switching losses and avoid fault turn-on of the device, it is very necessary to reduce the impact of CSI, especially in high di/dt applications.

Table 1 The influence of CSI on switching loss
(InnoGaN low-voltage product at 20A)

Value of CSI	Turn on energy(E_{on})	Turn off energy(E_{off})
L (CSI) = 0 nH	377nJ	163nJ
L (CSI) = 0.1 nH	533 nJ	275 nJ

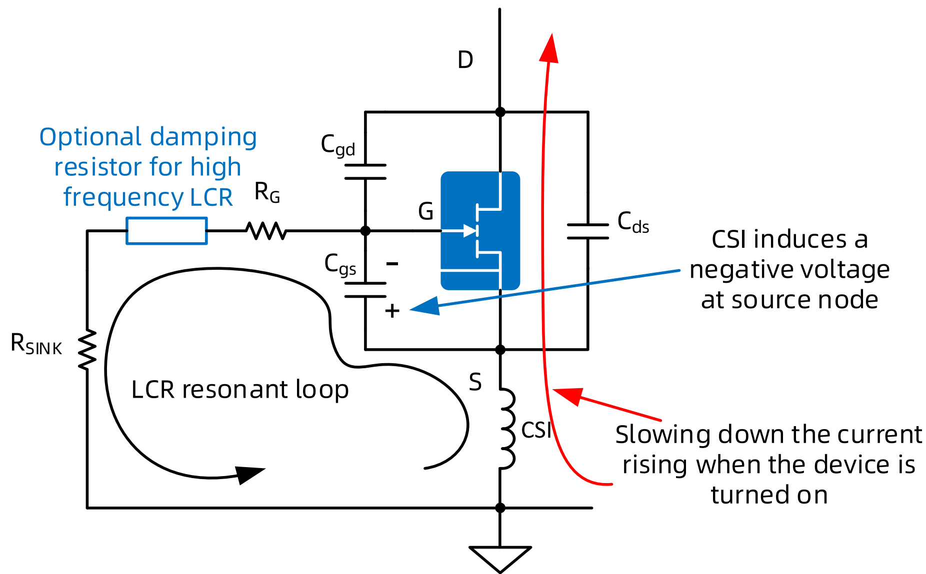

Figure 1 Schematic diagram of CSI in hard switching application

2.1.2. Optimization methods of CSI

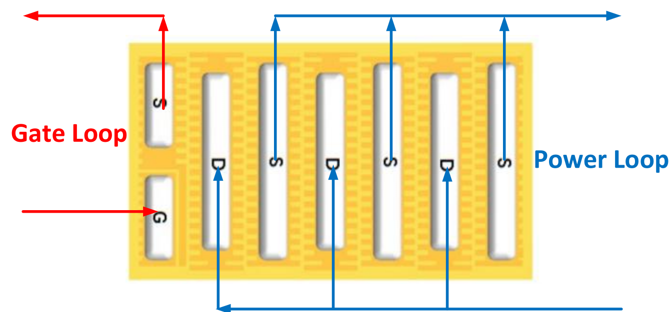

Figure 2 InnoGaN Schematic diagram of typical LV InnoGaN that separates the gate driving and power loops

1) For devices with Kelvin pins, such as high-voltage InnoGaN products in DFN and TOLL, Kelvin pin should be used to separate the gate driving loop and the power loop to avoid coupling.

2) For those without Kelvin pins, such as low-voltage InnoGaN products in QFN and WLCSP, Kelvin connection is still recommended to separate the gate driving loop and the power loop as shown in Figure 2. At the same time, the ground of the gate driving loop is connected to the Source terminal which is close to the Gate terminal through vias, to reduce the influence of CSI.

2.2. Gate driving loop

2.2.1. Impact of gate driving loop on performance of GaN

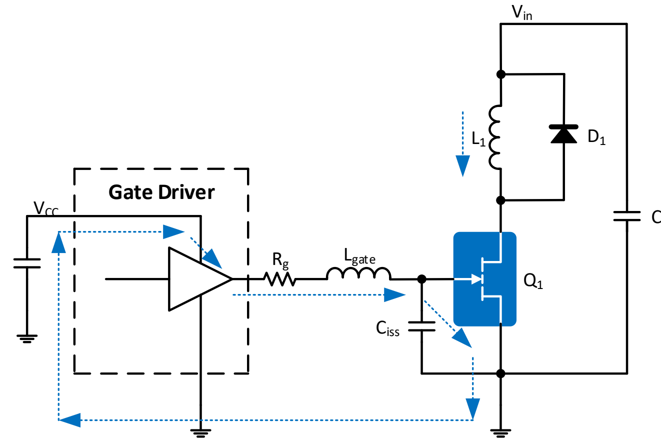

Figure 3 Schematic diagram of gate driving circuit for InnoGaN

Figure 3 shows the gate driving circuit of InnoGaN, which mainly consists of a gate driver IC, InnoGaN device, and loop parasitic inductance L_{gate}. During the switching process of the GaN device, the total resistance of the gate driving circuit will directly affect the performance of GaN device. If the gate resistance is too small, there will be large overshoot on the gate-source voltage V_{gs} and cause gate failure of the GaN device. Also if the ringing exceeds the threshold voltage V_{th} in off-state, it will cause fault turn-on and additional conduction loss. Although the overshoot and ringing on V_{gs} voltage can be eliminated with large gate resistance, but the transition process of the drain current will be significantly slowing down thus causing increased switching loss. Therefore, reducing parasitic inductance is the preferred solution.

2.2.2. Optimization methods for gate driving loop

1) In layout design, the gate driving loop and the power loop should be separated as much as possible, and the driver IC should be as close as possible to the GaN device;
2) The gate driving loop path should be as small as possible, while the forward and return paths should be overlaped and placed on the top and the adjacent inner layers, therefore reduce the gate driving loop

area and minimize parasitic inductance;

3) The total resistance of the gate driving loop should be small enough to ensure fast switching, and also large enough to prevent fault actions. The resistance value R_g should be set as following:

$$Rg \geq \sqrt{\frac{4 * L_{Gate}}{C_{iss}}} - R_{pullup}$$

*Note: R_{pullup} is the pull-up resistor inside the driver IC.

2.3. Power loop

2.3.1. Impact of power loop on performance of GaN

Since the current slew rate (di/dt) of GaN devices is much higher than that of Si MOSFETs, there wil be high voltage spikes on the drain-source voltage V_{ds} if the parasitic inductance on the power loop is not optimized. This may increase the power loss and the overvoltage risk of the devices. In addition, optimizing the parasitic inductance of the power loop also benefits the reduction of the impact of the power loop on the gate driving loop.

2.3.2. Optimization methods for power loop

1. Lateral power loop design

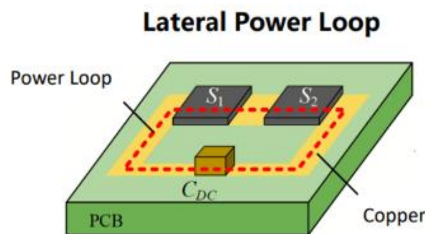

Figure 4 Lateral power loop design for InnoGaN

A lateral power loop layout is shown in Figure 4. The input capacitor and GaN device are located on the top layer of the PCB, and the area of the power loop is reduced by being close to each other. However, the reduction of the lateral power loop area is limited due to the clearance distance of devices in practical designs. Therefore, vertical power loop designs are recommended in order to minimize the loops, which will be demonstated in the next section.

2. Vertical power loop design

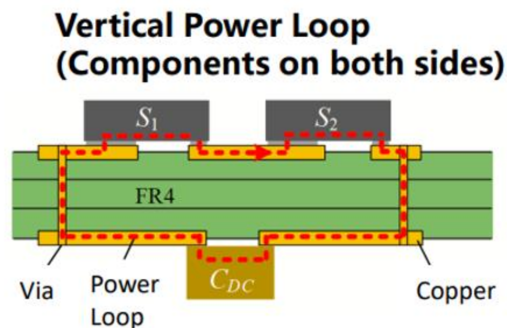

Figure 5 Example I of Vertical power loop design for InnoGaN

As shown in Figure 5, the GaN devices are placed on the same side of the PCB, and the DC bus capacitor is placed on the other side of the PCB. The current flows from the top layer through the device and through the vias to the capacitor on the bottom layer, and then back to the bottom layer forming the power loop. The power loop area is dependent on the thickness of the PCB in this design, which is smaller with smaller thickness.

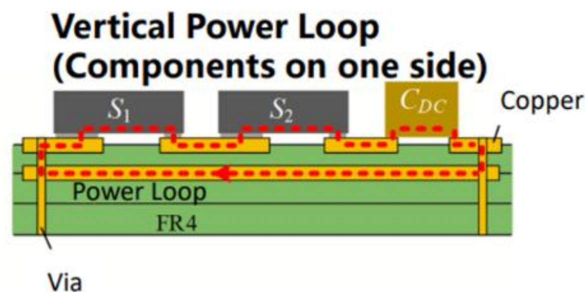

Figure 6 Example II of vertical power loop design for InnoGaN

The power loop could be further optimized as shown in Figure 6. In this design the GaN device and the input capacitor are placed on the same side of the PCB. The current flows through the inner layer of the PCB through the vias, and the current flow direction on the inner layer is opposite to that on the top layer, so the parasitic inductance can be reduced significantly by magnetic field cancelation. This design could achieve the minimum power loop area.

3. Layout design guidelines and procedures

3.1. Layout design guidelines

As mentioned in the previous sections, the CSI, power loop, and gate driving loop have an impact on the performance of GaN devices. Therefore, how to reduce the parasitic parameters from these three aspects is the key considerations in layout design for InnoGaN.

In addition, there are also other design considerations. For example, the coppers on the innerlayers between different nodes will introduce parasitic capacitance. The parasitic capacitance is connected equivalently to the drain and source nodes of the GaN devices, therefore leads to additional C_{oss}. . Similar coppers will also cause increased C_{iss} and C_{rss} across the devices. This will lead to additional switching losses and reduced the switching speed and performance of GaN. Especially in high-voltage hard switching applications , it may cause unnegligible losses.

In the layout design of GaN, we should try to follow the design principles as below:

1) CSI should be as small as possible. For devices with Kelvin pins, use the Kelvin source pins to reduce CSI. Kelvin source connection is also recommended for devices without Kelvin source pin.

2) Power loop area should be as small as possible. When the bulk-capacitor is relatively far from the high frequency loop, place MLCCs near the GaN devices.

3) The gate driving loop should be as small as possible. The driver ICs should be placed as close as possible to the GaN devices.

4) For both the gate driving loop and power loop, the current forward and return paths should be placed on adjacent layers and overlap each other, to create magnetic field self-eliminating and further reduce the loop inductance.

5) The gate driving loop and the power loop should be separate without overlap to avoid noise coupling from the power loop to the gate driving loop.

6) Minimize the parasitic capacitance formed by the drain and source

copper, especially in high-voltage hard-switching applications.

3.2. Layout design procedures

Similar as regular layout design procedures, several key steps in layout design with InnoGaN are device placement, wiring, copper laying, and thermal design.

1. Device placement

For different applications, layout is actually subject to certain restrictions due to product volume, space, and cost requirements. Nevertheless, for different applications and the device packages, the driving loop and power loop must be seperated in layout shown as Figure 7.

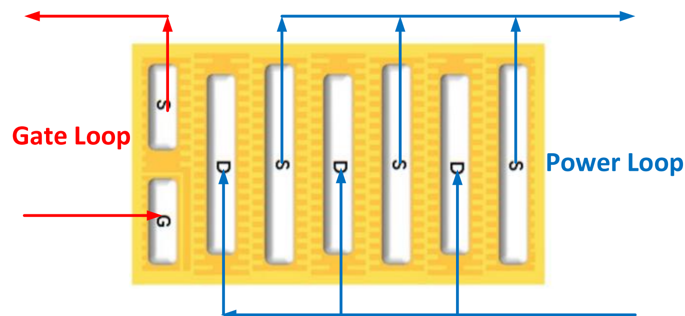

Figure 7 Gate driving loop and power loop direction for InnoGaN

In addition, as mentioned in the previous sections, there are also recommended layout methods for the power loop and gate driving loop to reduce the parasitic inductance. Taking low-voltage GaN as an example, the generally recommended PCB layout for low-voltage GaN synchronous BUCK applications is as follows: MLCC and high-side/low-side GaN are placed on the top layer of the PCB. MLCCs are close to the high-side GaN. The first layer is used for the placement of power devices, while the second layer is used to form the minimized power loop with magnetic field self-cancellation.

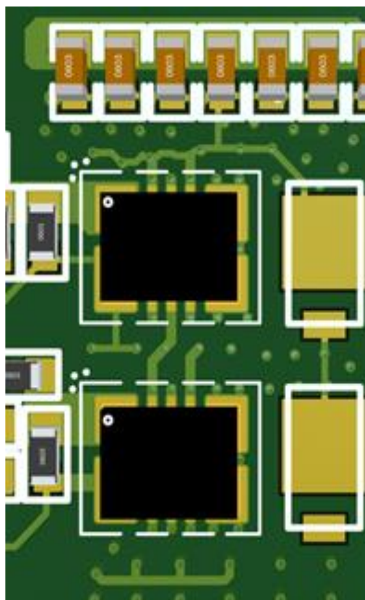

Figure 8 InnoGaN Recommended PCB layout (1)

Figure 9 InnoGaN recommended PCB layout (2)

2. Traces

The conventional design considerations should firstly be followed such as grounding, line length and width, , clearance distance, etc. Special attentions should be paid to the power loop and gate driving loop traces. It is recommended that after the wiring is completed, carefully check the wiring (length and area) of the gate driving loop and power loop according to the aforementioned principles and methods.

3. Copper laying

Copper laying is also very important in PCB design. Besides the current density, clearance distance, shielding of noise and interference, the influence of parasitic capacitance between different coppers and layers cannot be ignored. Especially in high-frequency hard switching situations, the C_{oss} of GaN devices accounts for a large proportion of the turn-on loss. In this case, the copper laying of the drain and source of the GaN devices needs to be

carefully optimized.

4. Thermal design

Thermal design runs through the entire PCB layout process. Attentions shoule be paid on the vias of the PCB. There are several suggestions as follows:

- The number of vias under the pad has a significant influence on the PCB thermal resistance. The via diameter of 0.4mm and the pitch of 0.85mm is recommended for TOLL and DFN8X8 packages.
- When there are vias under the pad, the density of vias outside the pad has little impact on the PCB thermal resistance. The diameter of external vias can be 0.3mm and the center distance is 1.5mm.
- The copper that extanded 2~4mm around the pad benefits the reduction of the PCB thermal resistance
- Solder-filled vias have a large impact on PCB thermal resistance, which is expected to reduce by 40%.
- Reducing the thickness of the PCB can reduce the PCB thermal resistance. The thermal resistance of PCBs with 1mm thickness is 40% lower than that of 2mm thickness., Thinner PCBs are preferred while the mechanical strength is within acceptable range.
- For packages with relatively small pads, such as FCQFN, the recommended via size is 0.3mm with 0.5mm outer diameter. The vias are not recommended to place directly on pads to ensure soldering quality. As the drain and source pads are relatively narrow, it is recommended to extend the pads with copper while within the safety clearance distance range. The interleaved vias could be place near the pads, which remains the copper in large area on bottom and inner layers to enhance the heat dissipation capability. A layout example with GaN in FCQFN package is shown in Figure 10.

Notes: For more details please refer to 《AN009-InnoGaN Thermal Design Guide》

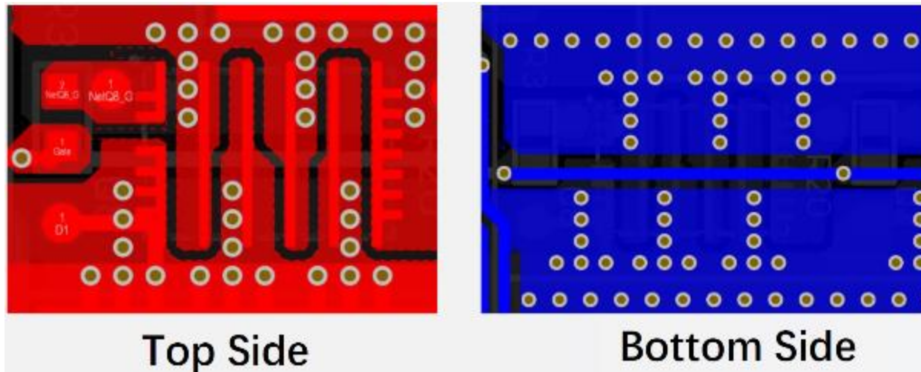

Figure 10 Diagram of via design for FCQFN package

4. Layout considerations for different packages

4.1. DFN

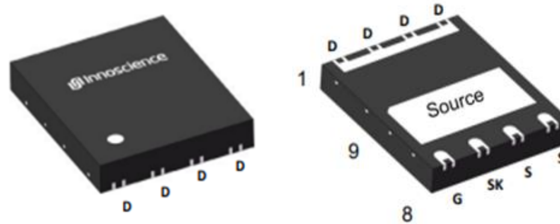

Figure 11 InnoGaN products in DFN package

InnoGaN products in DFN package are shown in Figure 11. Currently, InnoGaN products are available in DFN packaging in 5×6 and 8×8 sizes. Typical products include:

DFN5×6:

- INN700DA140C
- INN700DA190B
- INN700DA240B

DFN8×8:

- INN650D080BS
- INN700D140C
- INN700D190B

DFN is a standard package for power semiconductor devices, which is suitable for SMT. Both DFN5x6 and DFN8x8 are designed with Kelvin Source (SK) pins, and has the advantages of low parasitic parameters and thermal resistance.

It should be noted InnoGaN and traditional Si MOSFET are different in the layout that the pin definitions of DFN packaged. The comparison between these two is shown in Figure 12.

The thermal pad of Si MOSFET is usually connected to the drain. Since InnoGaN is a lateral structure device, the thermal pad of InnoGaN products is

connected to the source. The reduced area of the drain pad can reduce the area of the switching node, which is more EMC-friendly. The thermal pad is connected to the GaN substrate inside the package, which helps to effectively dissipate the heat generated internally and reducing the thermal resistance of the devices.

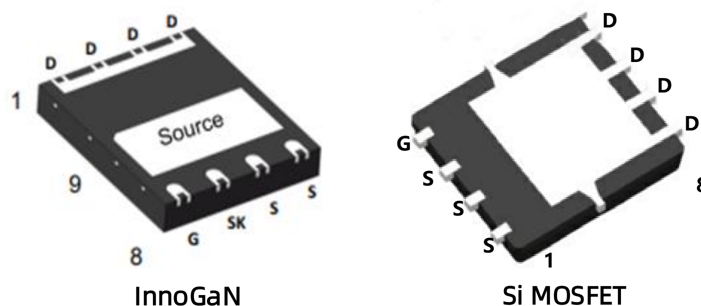

Figure 12 Comparison of InnGaN and Si MOSFET in DFN packages

4.2. TOLL

InnoGaN products using TOLL package are shown in Figure 13. Typical products include:

- INN650TA030AH
- INN650TA050AH
- INN650TA070AH

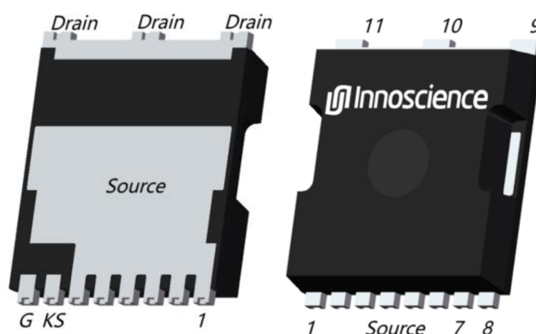

Figure 13 InnoGaN products in TOLL package

TOLL package is a standard package for power semiconductor devices and is suitable for SMT. It should be noted that the pin definitions of InnoGaN in TOLL package are different from the traditional Si MOSFET. The comparison between the two is shown in Figure 14.

Similar to the DFN package, the thermal pad of the Si MOSFET is connected to the drain, while the thermal pad of the InnoGaN product is connected to the source. Compared with Si MOSFET, the InnoGaN packaged in TOLL is designed with Kelvin Source (SK), which is more convenient to the optimize the gate driving circuit, reduces CSI and the coupling between the power loop and the gate driving loop.

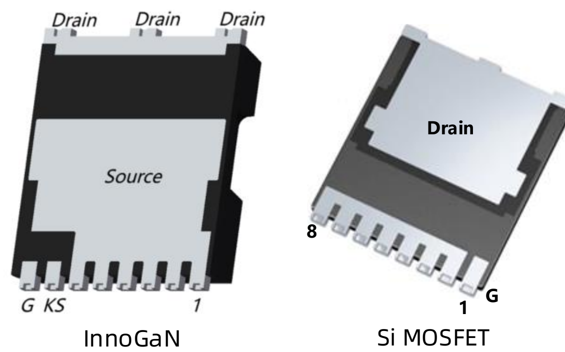

Figure 14 Comparison of InnoGaN and Si MOSFET in TOLL packages

4.3. WLCSP

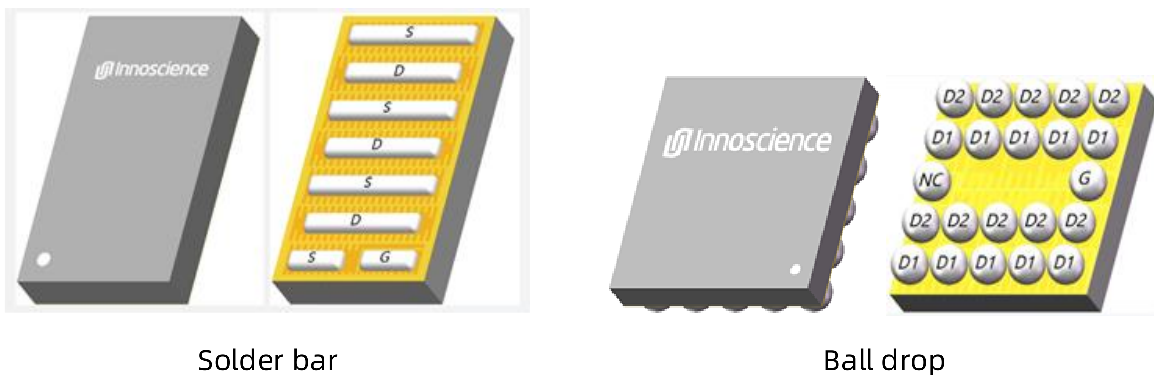

Figure 15 WLCSP packaged InnoGaN products

WLCSP (Wafer Level Chip Scale Packaging) is a wafer-level chip package, which effectively reduces the packaging size. Different from the traditional chip packaging method, WLCSP is first tested on the entire wafer, and then cut into discrete devices. InnoGaN products using WLCSP packaging include solder bar and ball drop, as shown in Figure 15.

The typical products include:

WLCSP (solder bar):

- INN100W032A

WLCSP (ball drop):

- INN040W048A
- INN040W080A
- INN040W120A

InnoGaN packaged in WLCSP is a surface mounted device, which has the advantages of small size, ultra-low parasitic parameters, and low thermal resistance. Drain and Source are usually designed in an alternating arrangement. In the layout design, it is recommended to use interleaved vias to minimize the parasitic parameters of the power loops.

4.4. FCQFN

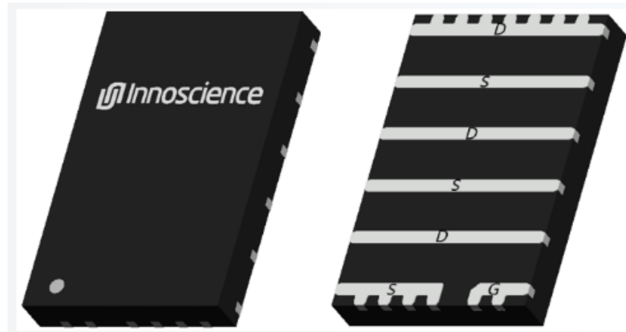

Figure 16 InnoGaN products in FCQFN package

InnoGaN packaged in FCQFN (Flip Chip Quad Flat No-lead) is shown in Figure 16. The typical products include:

- INN150FQ032A
- INN100FQ016A
- INN100FQ025A
- INN040FQ012A
- INN040FQ015A

The main features of FCQFN package are small size, small parasitic parameters, high packaging reliability, and easier for soldering. InnoGaN

products in FCQFN are usually designed with alternately arranged drain and source pads.The layout design method is similar to WLCSP.

4.5. TO package

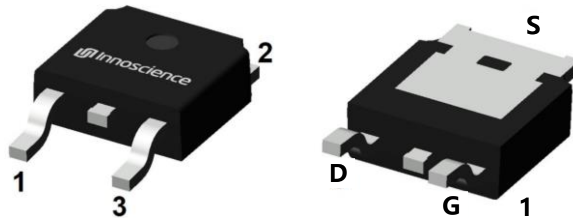

Figure 17 InnoGaN products in TO252 package

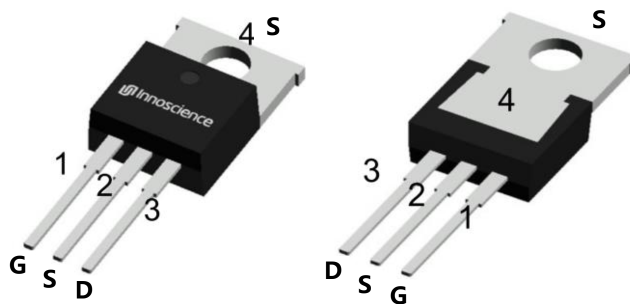

Figure 18 InnoGaN products in TO220 package

InnoGaN products in TO220 and TO252 packages are shown in Figure 17 and 18. The typical products include:

TO252:

- INN700TK140C
- INN700TK190B
- INN700TK240B
- INN700TK350B

TO220:

- INN700TH140C
- INN700TH190B

- INN700TH240B
- INN700TH350B

TO220 and TO252 are standard packages for power semiconductors. Different from Si devices, the back pad of GaN devices is connected to the source. In applications, this pad could be connected to a large area of copper or mounted on the heat sink to enhance the heat dissipation.

In the layout design, attentions should be paid to the different of pin definitions between InnoGaN and Si MOSFETs in TO220 and TO252 packages. The comparison between these two is shown in Figure 19. By exchanging the positions of drain and source, InnoGaN can more easily implement kelvin connections and enhance heat dissipation through layout.

Compared with DFN and other packages, package parasitic inductance of TO252 and TO220 is relatively larger. So more attention should be paid to the optimized the design of the gate driving loop and power loop, especially for the gate driving loop. The gate oscillation problem can be mitigated by adding ferrite beads of around 100R/100M to enhancing the reliability of the gate driving.

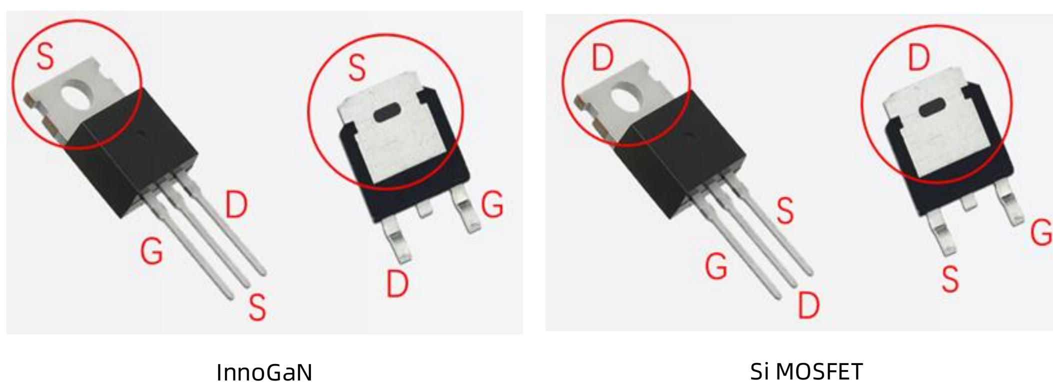

Figure 19 Comparison of InnoGaN and Si MOSFETs in TO220 and TO252 package

4.6. SolidGaN

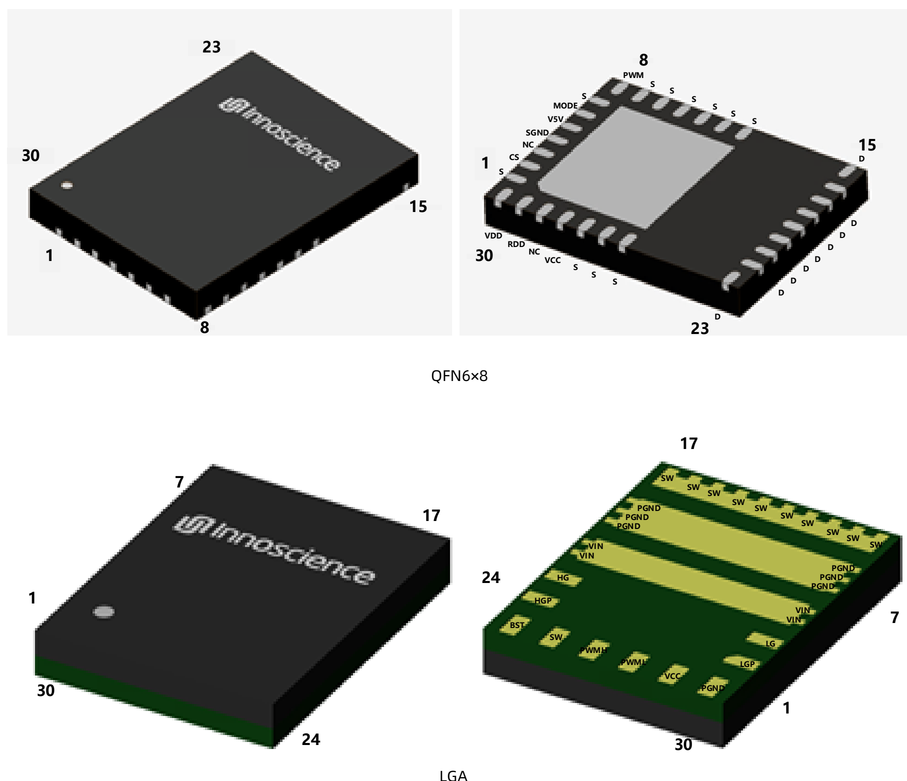

Figure 20 SolidGaN series products

SolidGaN products are shown in Figure 20. Currently, there are two packaging forms: QFN6×8 and LGA. Typical products include:

QFN6×8:

- ISG6102
- ISG6103

LGA:

- ISG3201

The SolidGaN series is an integrated design of GaN and driver IC. They are all surface mount packages and have optimized pin layout, which is more convenient to optimize layout design and minimize the loop parasitic parameters. Attention should be paid to ensure the signal traces do not overlap with the power loop to avoid noise interference. At the same time, large areas of copper are recommended to optimize heat dissipation.

5. Layout Design Examples

5.1. High voltage single-FET application

5.1.1. Layout considerations

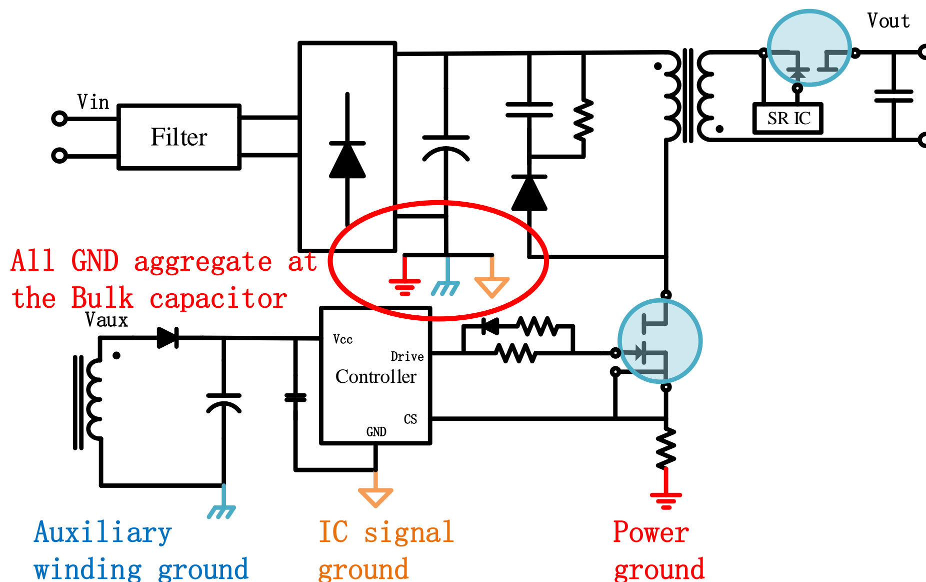

Figure 21 Schematic diagram of flyback circuit ground wire processing

The flyback topology is a typical application of high-voltage single-FET, commonly used in fast charger application. Whether for GaN or Si MOSFET, this topology requires special attention to the handling of the grounding. As shown in Figure 21, the auxiliary winding ground, IC signal ground, and power ground should be connected at the bulk capacitor to avoid noise interference in the IC ground and gate signal oscillation.

When applying GaN, the precautions below should be followed:

1) Due to the existence of the current sensing resistor, the Kelvin source pin of GaN should be directly connected to the source in this case, or the current sensing resistor will be bypassed.

2) The trace between the source terminal and the bulk capacitor ground should be as short and wide as possible to reduce the parasitic inductance L_s.

3) Seperate the gate driving loop and power loop to avoid interference and noise coupling.

4) The driver IC should be as close to GaN as possible to reduce the trace

length and and loop area.

5) In high-voltage applications, the parasitic capacitance of the GaN drain-source overlapping copper should be as small as possible to optimize switching loss.

5.1.2. Design example: PD fast charger

Figure 22 shows a layout example of DFN packaged high-voltage GaN in 65W fast charger solution.

Figure 22 3D overview of 65W fast charger Layout

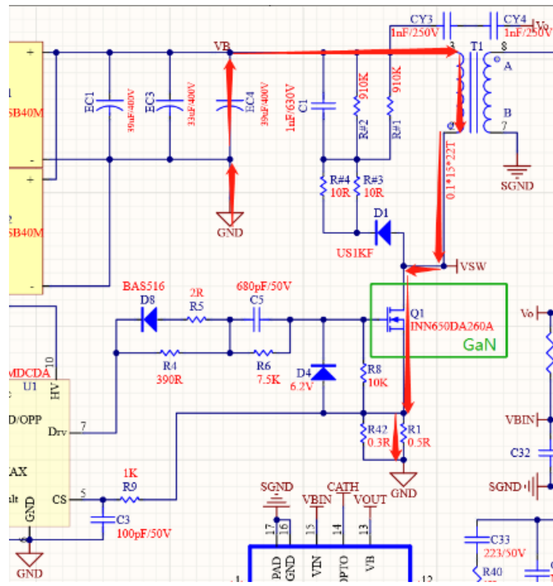

Figure 23 Schematic diagram of flyback primary side circuit

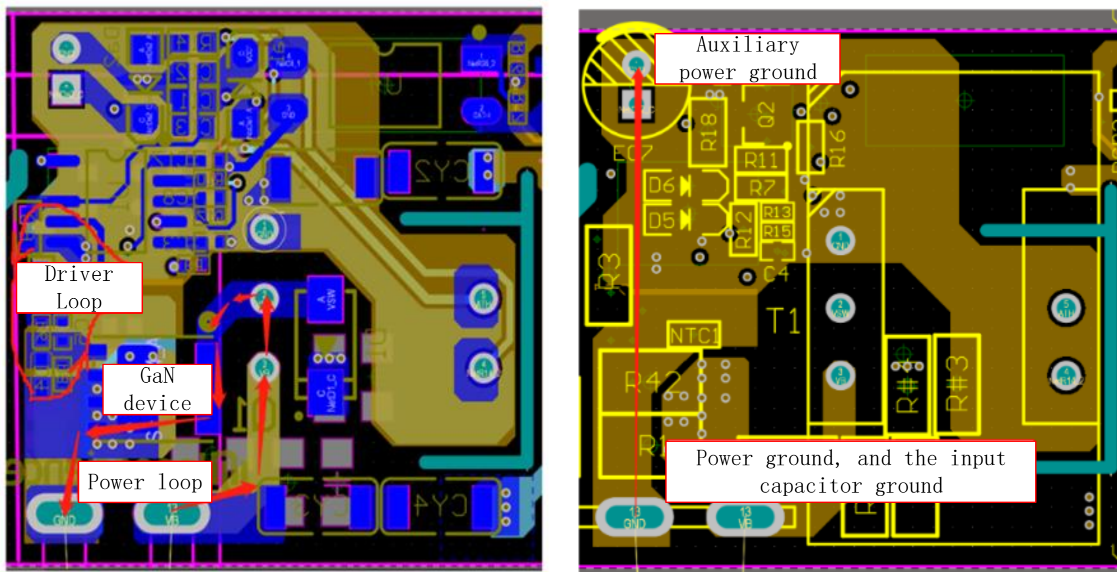

Figure 24 PCB layout of flyback primary side

In QR flyback topology, GaN cannot achieve zero voltage turn-on under high-grid. If the copper on the drain and source of GaN forms large parasitic capacitance, it will increase the turn-on losses. This problem is avoided in the layout in this case by separate the gate driving and power loops, as shown in Figure 24.

In addition, as can be seen from Figure 24, the ground of the auxiliary power supply and the power ground are connected through the wide copper in the inner layer.

5.2. High voltage half bridge application

5.2.1. Layout considerations

High-voltage half-bridge can be categorized as non-isolated and isolated application. One of the typical applications is PSU in data center. The two driving scenarios have slightly different layout precautions but are roughly the same. The considerations for layout in the two driving scenarios are generally similar.

For more details please refer to 《AN001-HV InnoGaN Gate Driving Design Guide》

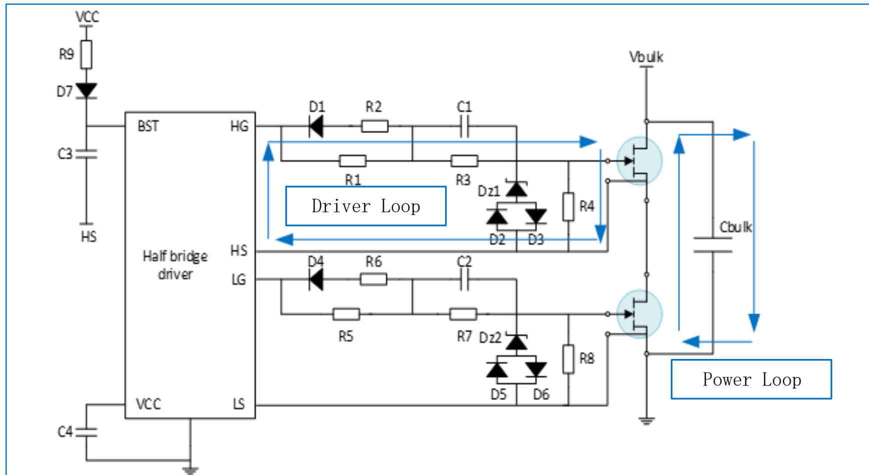

Figure 25 Half-bridge non-isolated gate driving circuit

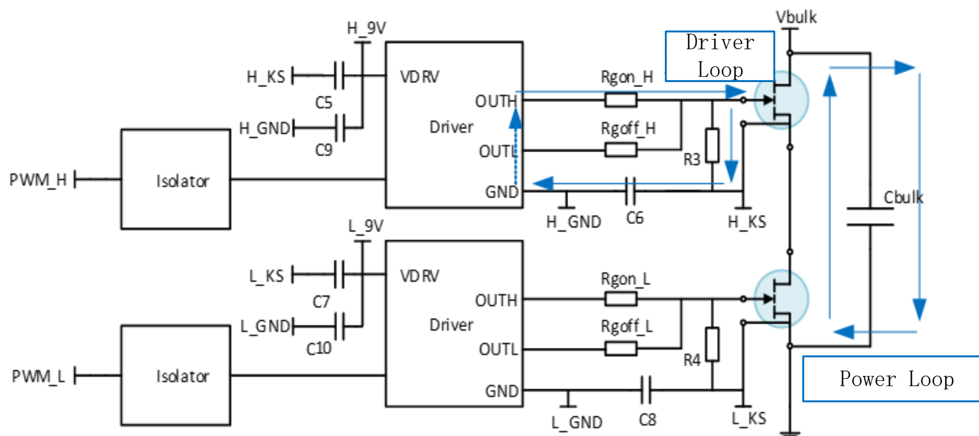

Figure 26 Half-bridge isolated gate driving circuit

The precautions for high voltage half bridge layout are as follows:

1) Bus MLCCs for decoupling should be close to the half-bridge GaN devices to reduce the power loop area formed by the high

side/low side GaN devices and the bus capacitor C_{bus}.

2) To minimize the PCB parasitic capacitance, the overlapping area between the switching node and the high-voltage DC bus as well as the power ground wire should be reduced. This reduction can effectively decrease the turn-on loss of GaN. For instance, in a four-layer layout design, the high-voltage DC bus and ground path can be arranged on the top Layer and the 1st mid layer, while the bottom layer can be configured at the switching node of this bridge. This setup serves to increase the distance and thereby reduce the parasitic coupling capacitance.

3) Use te Kelvin source connection to decouple the power loop and the gate driving loop to eliminate the influence of the power loop di/dt on the gate driving loop.

4) Reduce the gate driving loop. Place components on the top layer for drive signal routing. Place copper on the second layer to route the SK node so as to reduce the parasitic inductance of the gate driving loop. Increase the area of the SK node copper, which can effectively lower the inductance of the gate driving loop, and reduce the impact of noise coupling.

5) The gate driving circuits for the high side/low side devices of the half-bridge and the signal circuits of the driving ICs should be as independent as possible in space to prevent large parasitic capacitances among these loops from causing uncontrollable circulating currents between them.

5.2.2. Design example: PSU

Figure 27 is a design example of TOLL packaged high-voltage GaN in 2kW PSU application. More applications of PSU please refer to: Innosience Home - Applications - Data center

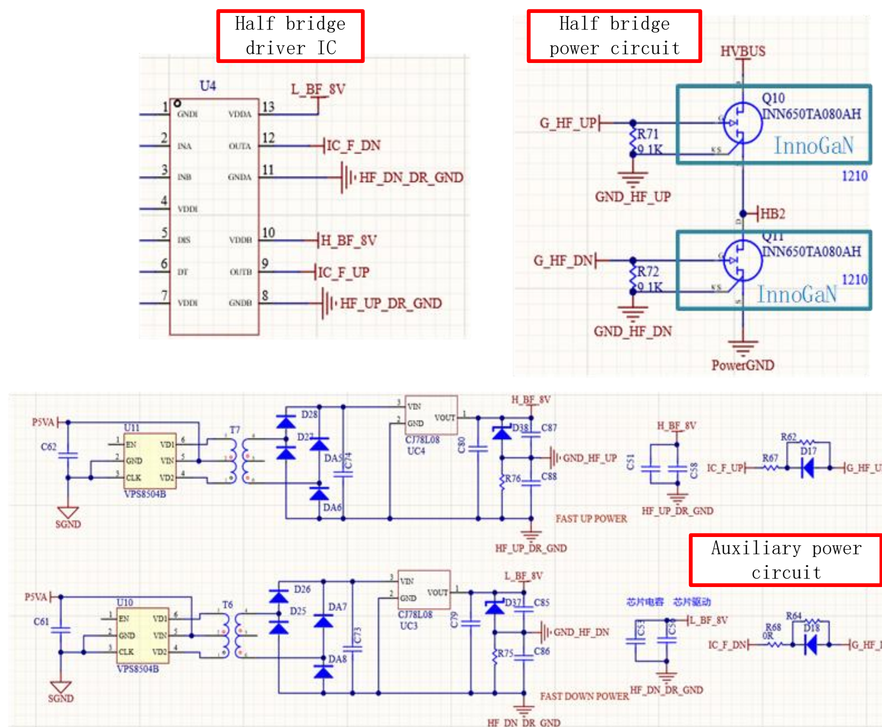

Figure 27 Schematic diagram of 2KW PSU - half-bridge power circuit

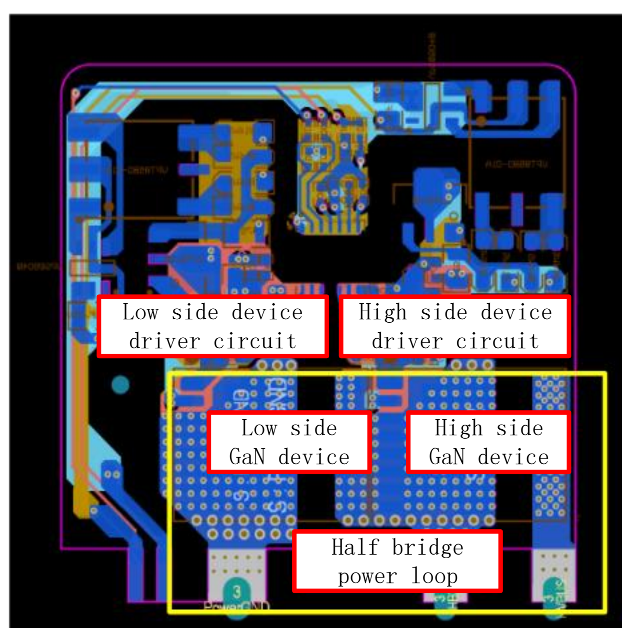

Figure 28 Half-bridge daughter board of 2KW PSU

This half-bridge module is a small card that is plugged into a mother board. It consists of a half-bridge power circuit with two GaN devices, driver IC and gate driving circuit, as well as the power supply of the gate driving circuits. The half-bridge topology works in hard-switching and generates losses both in turn-on and turn-off process. This could be considered as a typical layout example for high-voltage half-bridge circuits.

Due to volumn constraints in PSU applications, the high-frequency decoupling capacitor is placed close to the GaN half-bridge and placed on the mother board. The power loop and the gate driving loop are separated to avoid coupling. The switching node does not overlap with the high-voltage DC bus and power ground. The generation of parasitic capacitance is avoided. The Kelvin connection method is adopted for gate driving loop design. For more information, please refer to the application note AN001-High Voltage InnoGaN Driver Design Guide.

5.3. High voltage parallel application

5.3.1. Layout considerations

Base on the layout considerations for single-FET and half-bridge application, the following aspects need to be paid attention particularly to using GaN in parallel:

1) Reduce CSI and keep it as symmetrical as possible

2) Reduce the power loops and make them as symmetrical as possible

3) Reduce the gate loops and make them as symmetrical as possible

5.3.2. Design example: 300W adapter

Figure 29 shows a layout example of 300W adapter solution using DFN packaging high-voltage GaN. The front-stage is Boost PFC, and the 2nd-stage is half-bridge LLC. The front-stage are implemented with two GaN devices in parallel. For more information, please refer to Innosience Home - Applications - Consumer electronics.

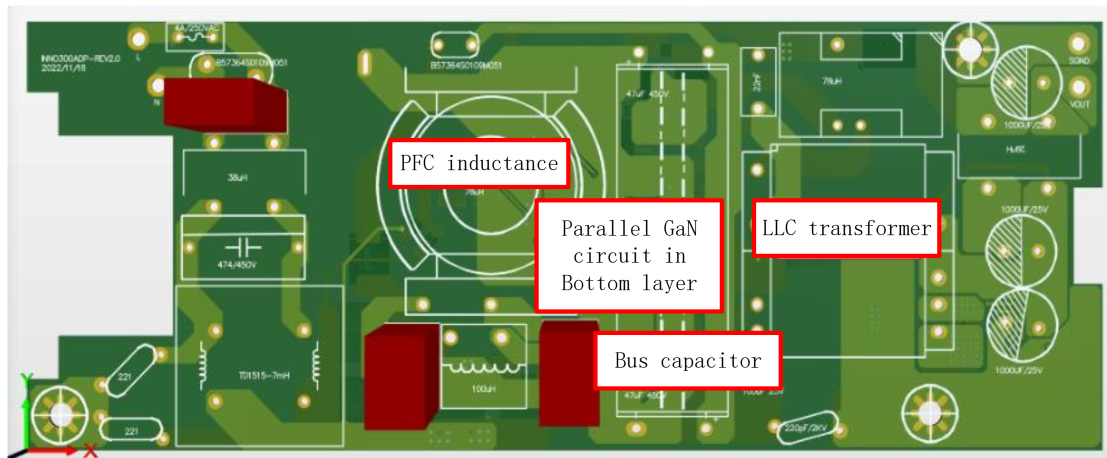

Figure 29 3D overview of 300W adapter layout design

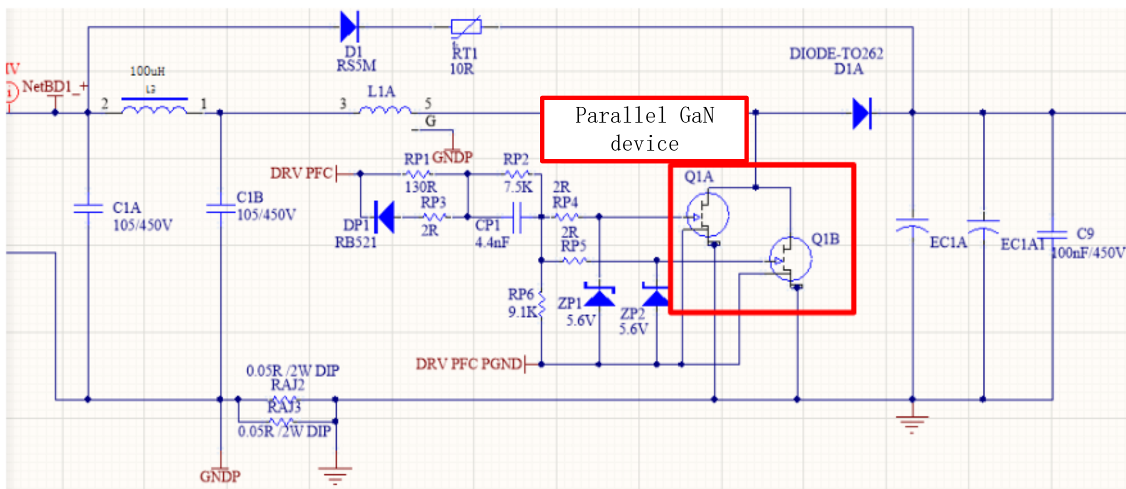

Figure 30 schematic diagram of PFC stage of 300W adapter

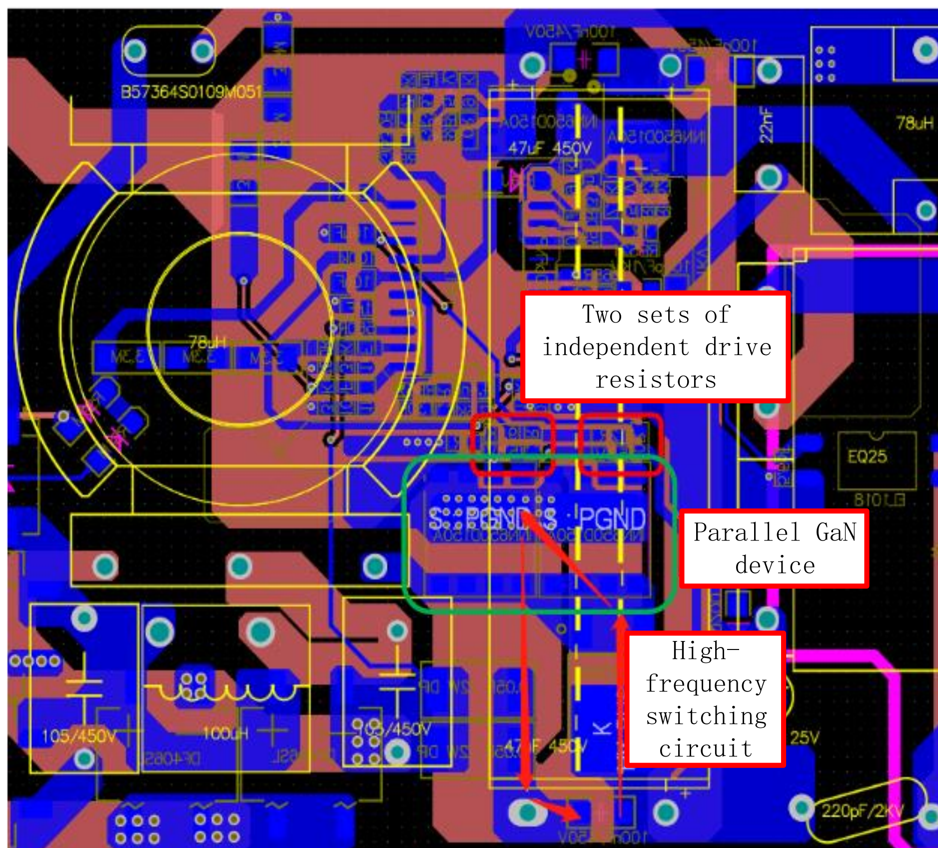

Figure 31 PCB layout of PFC stage of 300W adapter

As can be observed from the schematic diagram and the PCB layout, two parallelled high-voltage GaN transistors are symmetrically positioned. Also, the gate driving circuits share an RC network to generate the same drive signal. Moreover, two independent sets of gate resistors, GS pull-down resistors, and zener diodes, along with two sets of independent drive resistors, are also symmetrically arranged near the GaN devices.

In this layout design, the two paralleled high-voltage GaN transistors, the TO262 packaged freewheeling diodes and high-voltage MLCCs of the PFC stage the form a high-frequency current loop. The loop is short and small to reduce the parasitic inductance, which helps to reducing the V_{ds} spikes.

5.4. Low voltage single-FET application

5.4.1. Layout considerations

The flyback topology is also a typical application of low-voltage single-FET GaN. The layout considerations for high and low-voltage GaN in this situation are basically similar. Please refer to the high-voltage single-FET GaN section. The difference is that in low-voltage application, the V_{ds} voltage before GaN is turned on is not large, and the turn-on loss of the equivalent parasitic C_{oss} capacitance caused by copper is usually very small. Therefore, there is little need to pay extra attention to the drain and source overlap of copper (specifically depends on V_{ds} and switching frequency, a comprehensive balance); at the same time, low-voltage GaN packaging is conducive to reducing parasitic inductance on the PCB and improving flyback efficiency.

5.4.2. Design example: solar microinverter

Figure 32 shows a layout example of a 2kW solar microinverter using FCQFN package low-voltage GaN. The front stage uses flyback topology to realize voltage step-up. The primary GaN transistors of flyback is realized by two low-voltage GaN in parallel. GaN is placed on the bottom layer of the PCB

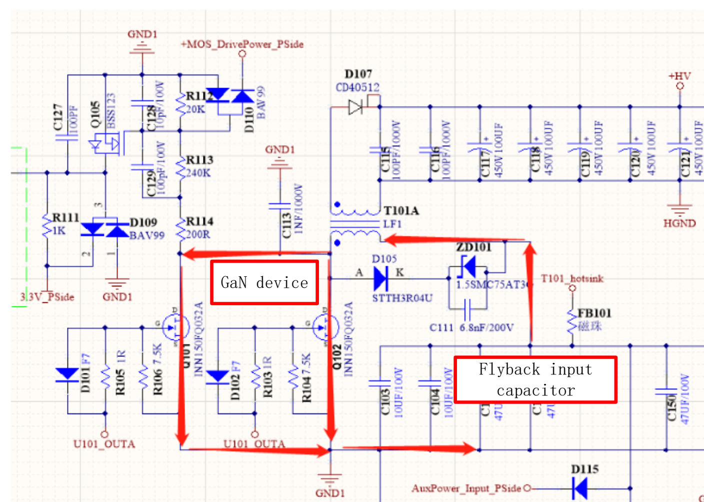

Figure 32 Partial schematic diagram of solar microinverter

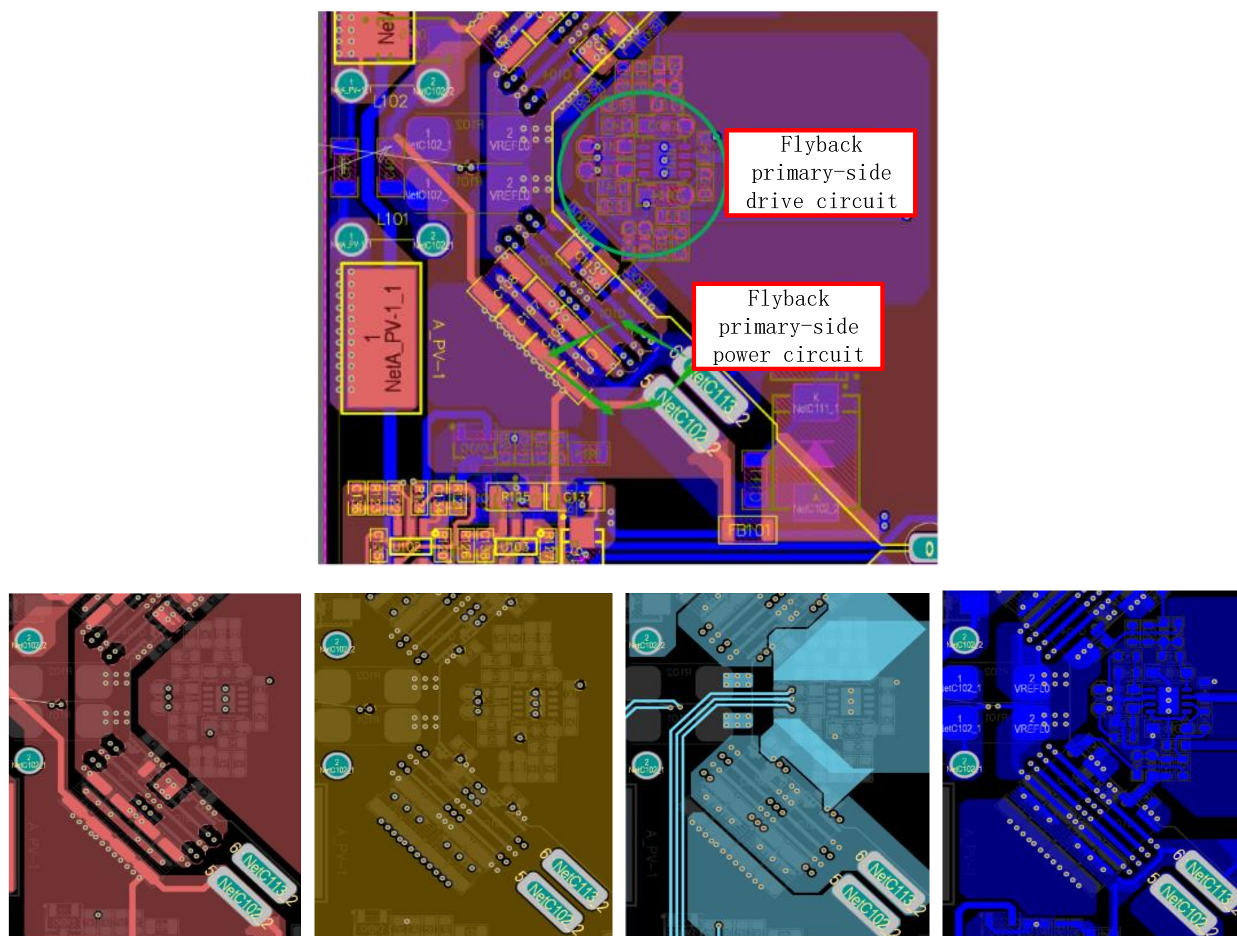

Figure 33 PCB layout of solar microinverter

In this design, the primary loop of each flyback is composed of a 1210 MLCC, the primary winding of flyback transformer, and two parallel GaN transistors. Several 1210 MLCCs connected in parallel are placed on the top layer of the PCB. The second layer is routed as the power ground. The third layer is the drain of GaN , which is connected to the transformer winding, and the copper between the transformer and the MLCC. Low-voltage GaN transistors are placed on the bottom layer of PCB. This layout method reduces the area of the power loop and the parasitic inductance as much as possible.

The gate driving circuit is placed on the other direction, and the kelvin source connection is formed on the source pins closest to the gate pin through vias. The ground of the gate driving circuit is connected to the via (power ground) at a single point to reduce the influence of CSI.

5.5. Low voltage half bridge application

5.5.1. Layout considerations

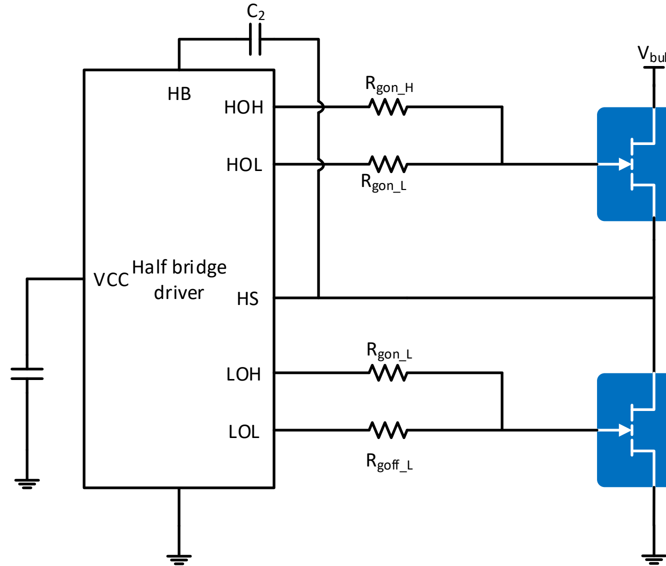

Figure 34 Half-bridge non-isolated gate driving circuit

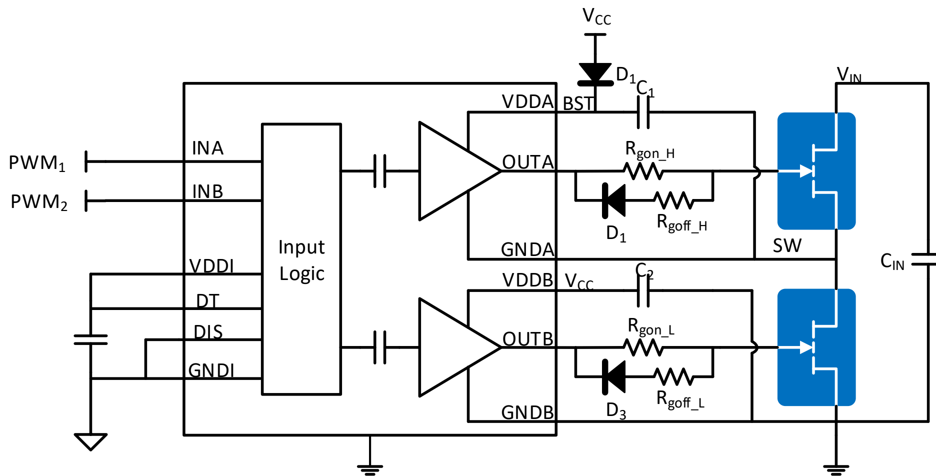

Figure 35 half-bridge driver circuit with integrated digital isolation

There are many typical applications for low-voltage half-bridges, such as synchronous BUCK, LLC power module , etc. The design of low-voltage half-bridge is similar to the high-voltage half-bridge, which is also divided into non-isolated and isolated applications. In summary, the key precautions are as follows:

1) The V_{CC} power supply capacitor should be close to the driver IC pin, to reduces the turn-on loop and the oscillation on power supply;

2) In order to reduce the loop inductance, the driver should be as close as possible to GaN to reduce the parasitic inductance in the gate driving loop;

3) Reduce the overlap between the gate driving and power loops and reduce the CSI;

4) The half-bridge bootstrap capacitor needs to be close to the driver IC pins, and the gate driving and power loops need to be separated to reduce the impact of the power circuit dv/dt on the gate driving loop.

The layout of low-voltage GaN exhibits certain disparities when compared to that of high-voltage GaN. The operating frequency of low-voltage GaN is usually extremely high, often reaching into the MHz range. At such high switching frequency, in order to fully exploit the advantages proffered by GaN, particular attention must be dedicated to the layout to minimize the parasitic inductance engendered by the PCB layout.

5.5.2. Design examples: 48V power module

Figure 36 shows a layout design example of 1KW 48V to 12V power module with SolidGaN in LGA package (ISG3201, monolithic package integrating half-bridge and drivers). For more information about 48V to 12V power module, please refer to Innosience Home - Applications - Data center.

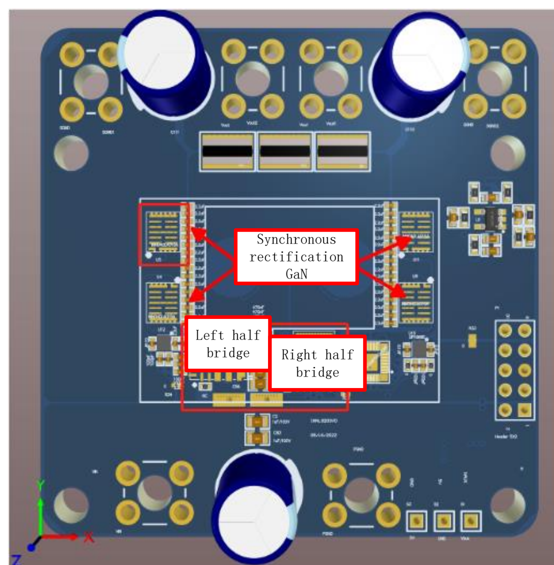

Figure 36 3D overview of 48V power module

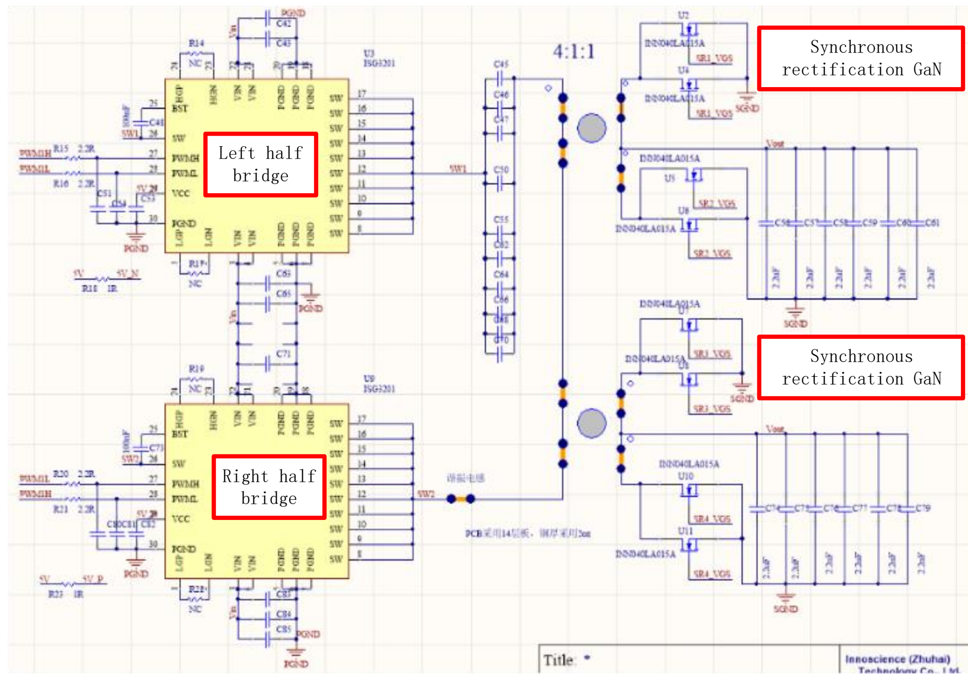

Figure 37 Schematic diagram of 48V power module

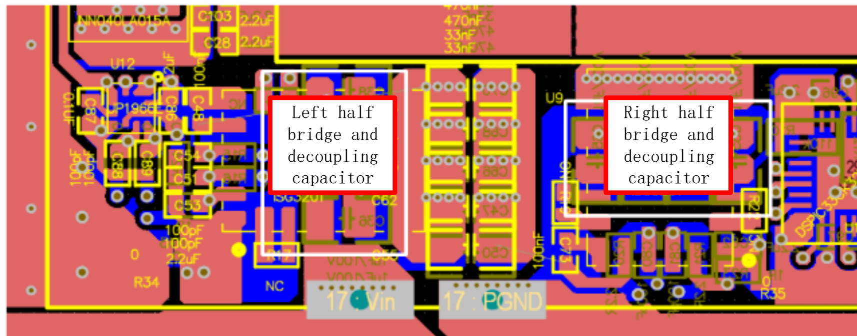

Figure 38 Layout of primary side half-bridge circuit

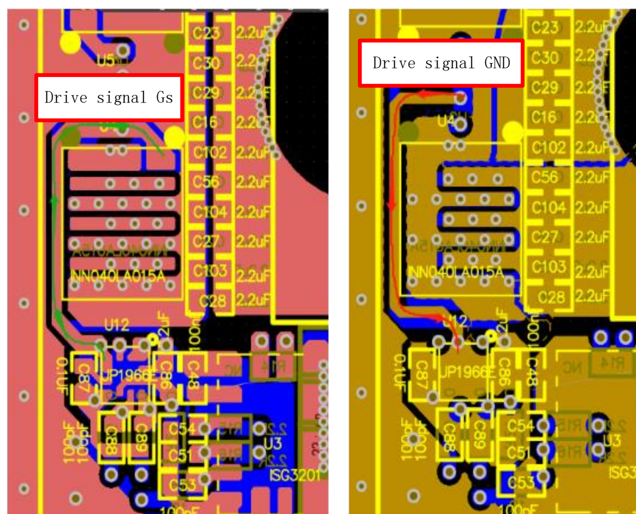

Figure 39 Layout of secondary side SR circuit

The 48V module is a full-bridge LLC topology. The primary side is composed of two pieces of ISG3201 to form two half-bridge bridge arms. Each synchronous rectifier (SR) transistor on the secondary side is realized by two pieces of INN040FQ015A connected in parallel. Each ISG3201 integrates the high side/ low side transistors and a half-bridge driver. The circuit is simple and easy for design.

In this design example, ISG3201 is placed on the top layer, and the DC decoupling capacitors are placed on the bottom layer directly below ISG3201. Multiple vias are used to directly connect them, minimizing the power loop parasitics. As for the gate driving of the secondary side SR GaN, the traces on top and inner layers almost completely overlaps, reducing the loop area and parasitic inductance as much as possible.

5.6. Low voltage parallel application

5.6.1. Layout considerations

Similar to high-voltage GaN, low-voltage GaN devices in parallel applications also need to pay attention to the following aspects compared with single FETs:

1) Reduce CSI and keep in symmetry
2) Reduce the power loop and keep in symmetry
3) Reduce the gate driving loop and keep in symmetry

The difference is that low-voltage GaN will run at higher switching frequencies, such as several MHz. Symmetry in layout becomes more important paralleled low-voltage GaN transistors. Figure 40 shows the recommended layout method for paralleled low-voltage GaN for both single FET and half-bridge applications. For more details please refer to AN004-InnoGaN Parallel Design Guide.

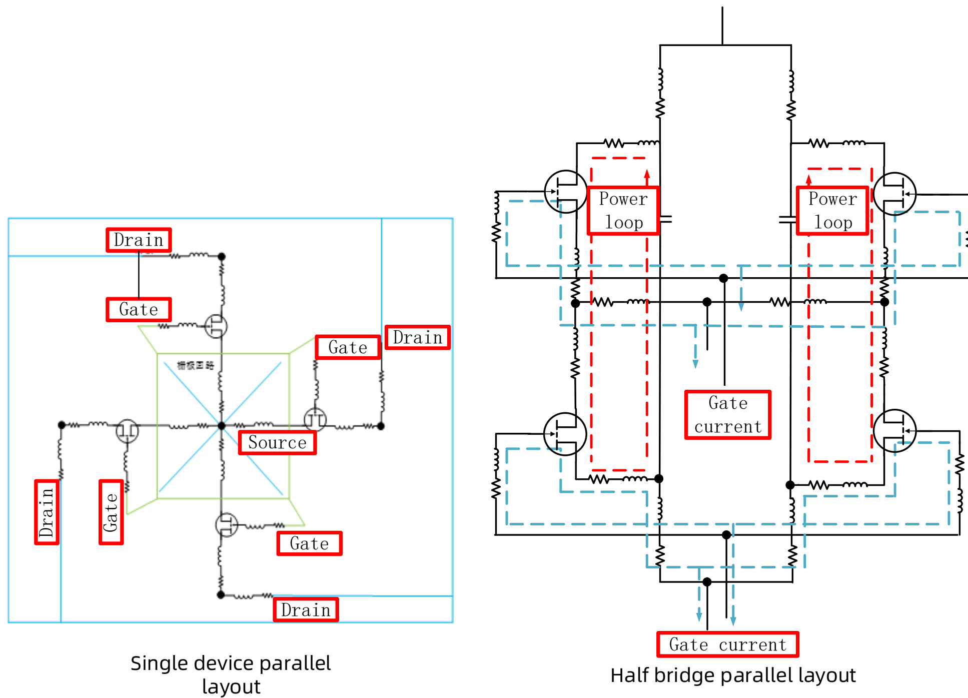

Figure 40 Layout Methods for paralleled low-voltage GaN

5.6.2. Design example: buck-boost module

Figure 41 and 42 show a layout design example of a 1kW Buck-Boost solution with low-voltage GaN in FCQFN package.

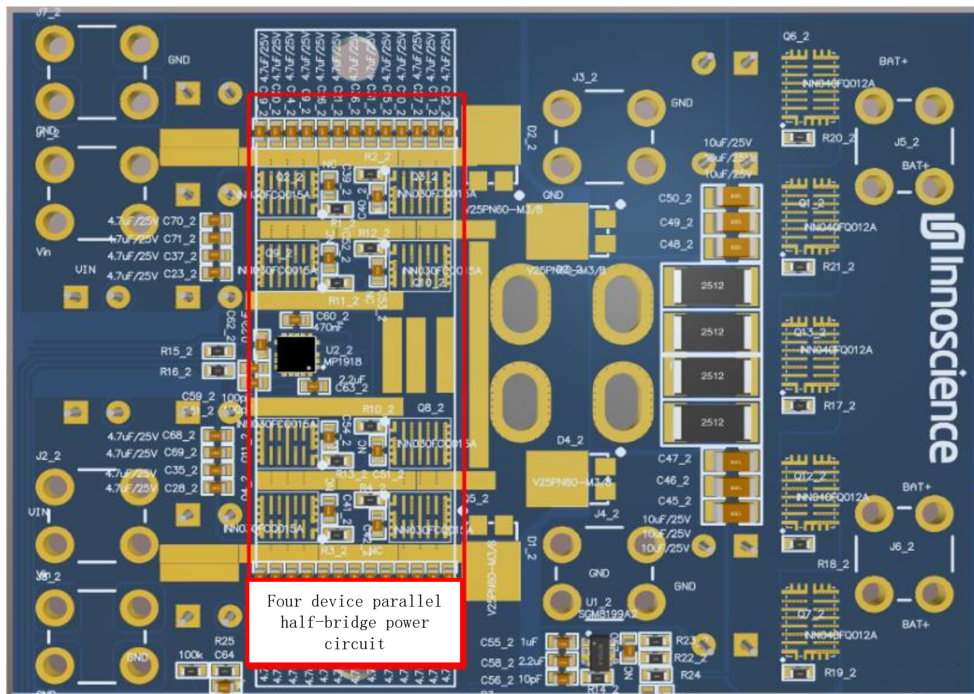

Figure 41 3D overview of buck-boost module

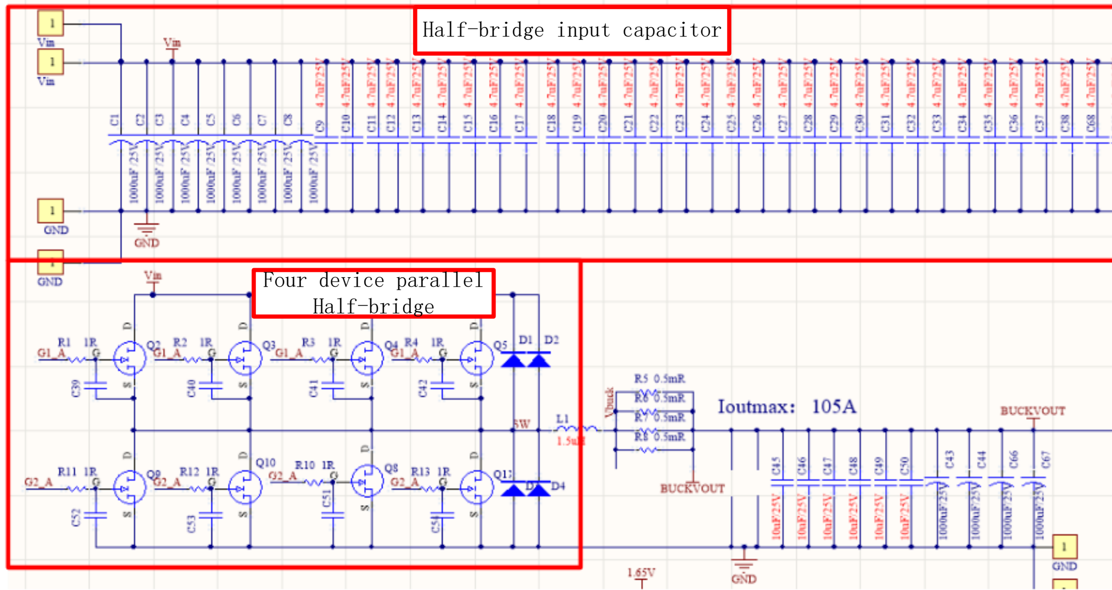

Figure 42 Schematic of buck-boost module

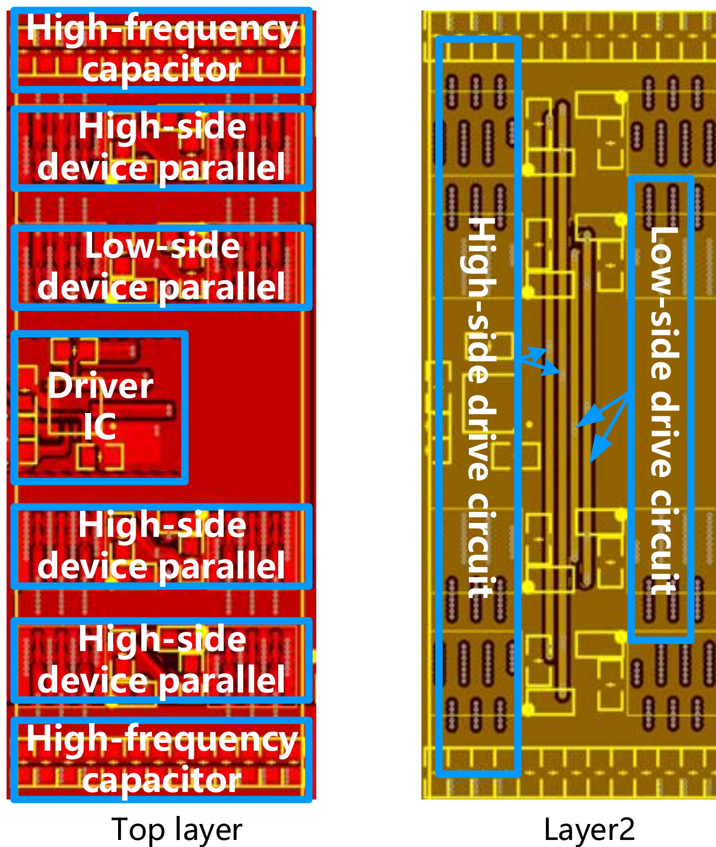

Figure 43 Top and 2nd layers of buck-boost module

As can be seen from the top layer, the layout is in symmetrical configuration both vertically and horizontally with the driver IC as the midpoint. The two paralleled GaN transistors are also symmetrically placed

in horizontal direction. At the same time, each set of half bridge have a group of MLCCs nearby, which effectively reduces the parasitic parameters in the power loops. The ground of the gate driving circuit is connected to the source node of GaN through a single via to reduce CSI while ensuring the symmetry of the gate driving loops. In addition, the copper of the power ground is laid on the second layer to form a high-frequency loop with the top layer with magnetic cancellation.

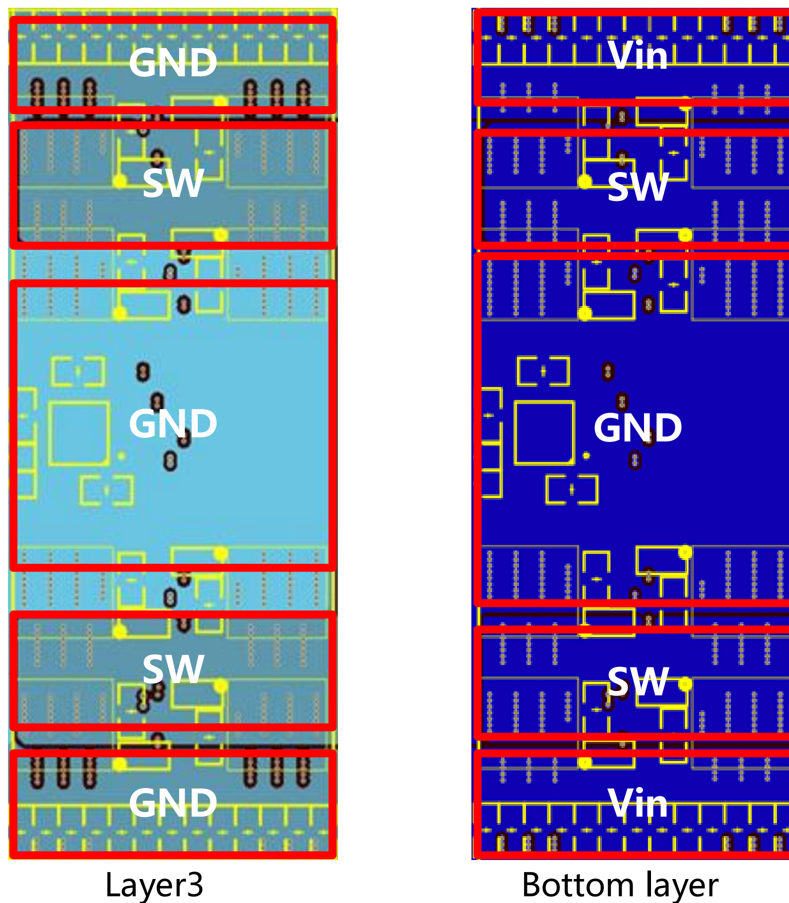

Figure 44 3rd and bottom layers of buck-boost module

The third layer and the bottom layer are shown in Figure 44, which mainly provide wide paths for high current and optimized heat dissipation.

Revision History

Date	Version	Description	Author
2024/02/07	1.0	English Translation	AE team
2024/12/19	1.1	Update pictures, add hyperlink	AE team

Note: There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death. Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end- user equipment.

Reminder:This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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